

# **Addendum for Operation Manuals**

## **SPI Protocol**

### **Matrix SPI Displays**

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## 1 Message frame

**Table 1. SPI message frame**

SOF	Command	[Address]/Data	Check	EOF
"1111 1111" (FF <sub>h</sub> )	8 bits	N x 8 bits	XOR	"0101 0101" (55 <sub>h</sub> )

SOF (Start of Frame) is the only byte where MSB is '1'. All other byte the MSB is '0'.

## 2 Row number

Row number are needs with some commands. Row address is 14 bits long carried inside a 16-bit word.

**Table 2. Row number to address table**

Row number	Address															(hex)	
	0	B13	B12	B11	B10	B9	B8	B7	0	B6	B5	B4	B3	B2	B1		B0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	00 <sub>h</sub> 01 <sub>h</sub>
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	00 <sub>h</sub> 02 <sub>h</sub>
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	00 <sub>h</sub> 03 <sub>h</sub>
...																	...
127	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	00 <sub>h</sub> 7F <sub>h</sub>
128	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	01 <sub>h</sub> 00 <sub>h</sub>
129	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	01 <sub>h</sub> 01 <sub>h</sub>
...																	...
238	0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	0	01 <sub>h</sub> 6E <sub>h</sub>
239	0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	1	01 <sub>h</sub> 6F <sub>h</sub>
240	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	01 <sub>h</sub> 70 <sub>h</sub>

### 3 SPI protocol

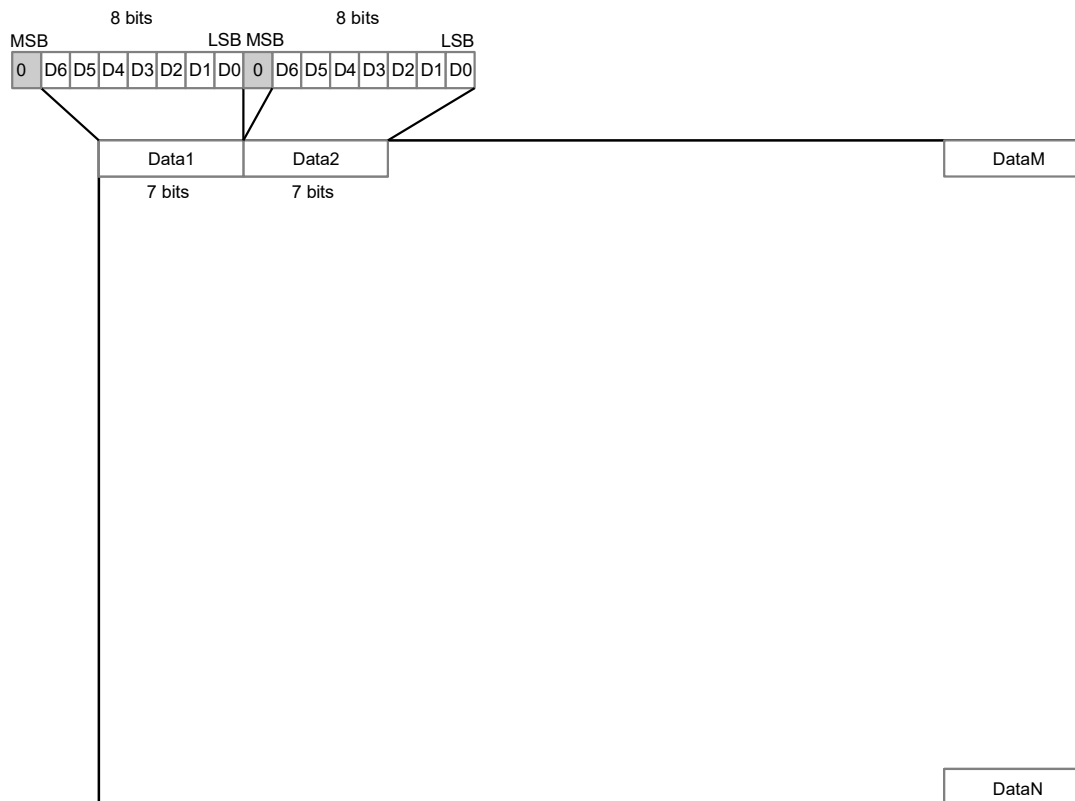
#### 3.1 Commands

Command	Hex #	Binary							
Write complete display data	01 <sub>h</sub>	0	0	0	0	0	0	0	1
Write display block (multiple rows)	02 <sub>h</sub>	0	0	0	0	0	0	1	0
Write one row	04 <sub>h</sub>	0	0	0	0	0	1	0	0
Clear screen (full black or full transparent)	19 <sub>h</sub>	0	0	0	1	1	0	0	1
All pixels ON (full yellow)	1A <sub>h</sub>	0	0	0	1	1	0	1	0
Invert display image	1C <sub>h</sub>	0	0	0	1	1	1	0	0
Write frame frequency	61 <sub>h</sub>	0	1	1	0	0	0	0	1
Communication period	62 <sub>h</sub>	0	1	1	0	0	0	1	0

#### 3.1.1 Write complete display data

Pixels are going from left to right from top to bottom. A first pixel in a byte is the most significant one. See Figure 1 for reference.

Command	Data1 ... DataN			Check
01 <sub>h</sub>	<b>Data1</b> 8bits	----	<b>DataM</b> See Equation 1	Xor(Command,Data)
	<b>DataM+1</b> 8bits	----	<b>Data</b> See Equation 1	
	-	-	-	
	<b>Data</b> 8bits	----	<b>DataN</b> See Equation 1	



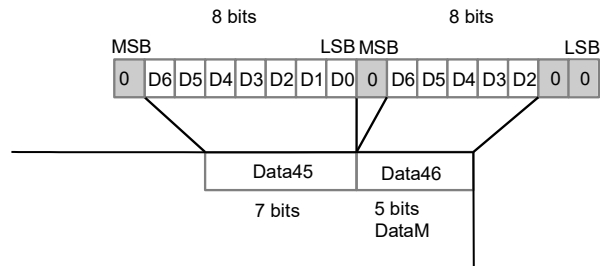
**Figure 1. Display pixel locations on image data mapping.**

Each row of data should be 8 bits divisible. If the last byte of row doesn't not fill up with the display data, the required number of '0' is appended to the end of the bytes. The needed '0' bits end of the last row byte (DataM) can be calculate:

$$7 - (\text{Columns} - (\text{INT}(\text{columns} / 7) * 7)).$$

**Equation 1. Row last byte '0' fill up calculation**

E.g. EL320.240 display have 320 columns each row. So the needed '0' will be 2 [7-(320 - INT(320/7)\*7)) = 2].



**Figure 2. An example of generating the last byte of row on EL320.240 display.**

### 3.1.2 Write display block (multiple rows)

Command	First row address	Last row address	First bits first row	----	Last bits of last row	Check
02 <sub>h</sub>	16 bits See <b>Error!</b> <b>Reference source not found.</b>	16 bits See <b>Error!</b> <b>Reference source not found.</b>	8 bits	8 bits	8bits See Equation 1	Xor(Command, Address,Data)

### 3.1.3 Write one row

Command	Row address	First bits of row	----	Last bits of row	Check
04 <sub>h</sub>	16 bits See <b>Error!</b> <b>Reference source not found.</b>	8 bits	8 bits	8bits See Equation 1	Xor(Command, Address,Data)

### 3.1.4 Clear screen (full black or full transparent)

Command	Check
19 <sub>h</sub>	Xor(Command,00 <sub>h</sub> )

Fill the display frame memory with '0'.

### 3.1.5 All pixels ON (full yellow)

Command	Check
1A <sub>h</sub>	Xor(Command,00 <sub>h</sub> )

Fill the display frame memory with '1'.

### 3.1.6 Invert display image

Invert command only inverts visible display picture and does not manipulate picture data on display frame memory. Consecutive invert commands toggle displayed image between inverted and non-inverted mode.

Command	Check
1Ch	Xor (Command,00h)

### 3.1.7 Write frame frequency

Relative Luminance	Command	Data	Check
100% <sup>1)</sup>	61h	01h	Xor (Command,Data)
75%	61h	02h	Xor (Command,Data)
50%	61h	04h	Xor (Command,Data)
30%	61h	08h	Xo r(Command,Data)

Notes: <sup>1)</sup> Default luminance

### 3.1.8 Communication period

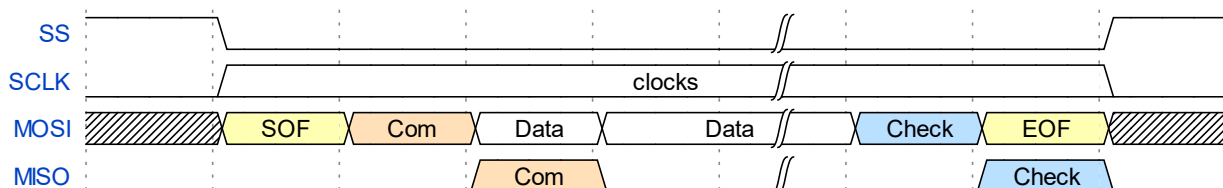
Display expects host to communicate periodically. If display does not receive a valid frame within a time period of 1.5 seconds, the display is cleared to indicate that integrity of SPI bus may have been compromised or host system has malfunctioned. This function can be disabled.

Communication period	Command	Data	Check
1,5 sec <sup>1)</sup>	62h	01h	Xor (Command, Data)
Disabled	62h	7Fh	Xor (Command, Data)

Notes: <sup>1)</sup> Default time period

## 3.2 Display responding (MISO signal)

MISO signal definition is added for possible future updates. Currently it is not implemented.



**Figure 3. MISO Signal**

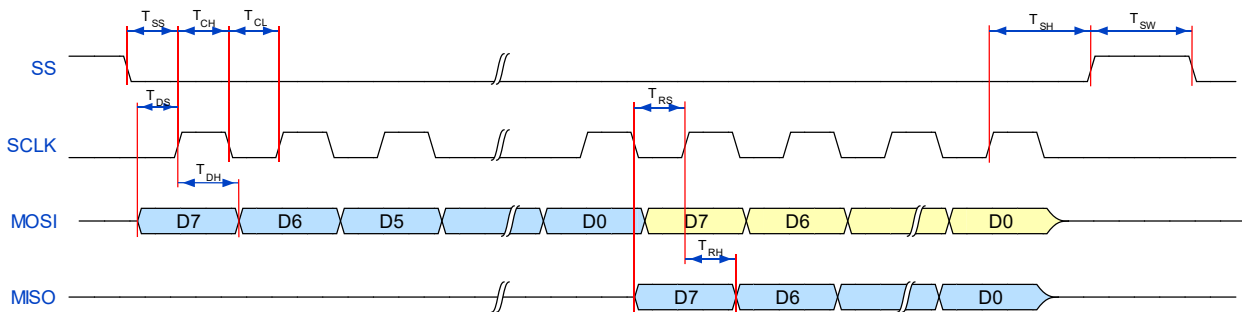
### 3.3 SPI timing

The SPI is driven with the rising edge of SCLK. A falling edge on SS signal indicates the beginning of an access on the SPI, the rising edge of SS signal ends an access on SPI. An access must consist of exactly 8 bits for write operation.

It is preferable to keep SS signal constantly active throughout the entire write operation. Display can continue the transfer if SS signal is momentarily driven to inactive state for short period of time. Successful continuation requires that clock pulse count and bit-based byte count remain in sync during the glitch.

The SPI interface Clock polarity (CPOL) and clock phase (CPHA) are 0. At CPOL=0 the base value of the clock is zero for CPHA=0 and data are captured on the clock's rising edge (low to high transition) and data is propagated on a falling edge (high to low clock transition).

The timing restrictions on SPI are defined in Figure 4 and Table 2:



**Figure 4. Video input timing diagram**

**Table 2. Timing restrictions**

Description	Symbol	Minimum	Maximum	
SCLK frequency			5	MHz
SCLK high time	$T_{CH}$	100		ns
SCLK low time	$T_{CL}$	100		ns
SS -> SCLK setup time	$T_{SS}$	100		ns
SCLK -> SS hold time	$T_{SH}$	100		ns
SS disabled between cycles	$T_{SW}$	200		ns
Data setup time	$T_{DS}$	60		ns
Data hold time	$T_{DH}$	60		ns
Response Data setup time	$T_{RS}$	90		ns
Response Data hold time	$T_{RH}$	90		ns



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